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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,951	11/10/2003	Wei-Hung Huang	MTKP0092USA	2950

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EXAMINER	
MOLL, JESSE R	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,951	HUANG ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/2/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

Acknowledgment of papers filed: amendment on 21 May 2006. The papers filed have been placed on record.

Drawings

2. The drawings were received on 21 May 2006. These drawings are acceptable.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objections to claims 3, 4 and 10. The objections are respectfully withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Catherwood (U.S. Patent No. 6,976,158 B2).

6. Regarding claim 1, Catherwood discloses a microcomputer apparatus comprising: a processing unit (execution units 115; see fig. 1) for executing instructions; and a loop counter (repeat count register; see col. 2, lines 64-66) coupled to the processing unit (all components in a processor are coupled) for receiving and storing a loop count value (see col. 8, lines 59-60) according to a loop instruction (see col. 8, lines 60-62) executed by the processing unit (instruction are all executed by the execution unit); wherein the processing unit decrements the loop count value stored in the loop counter (see col. 9, lines 1-2) each time an instruction is looped (see col. 9, lines 8-11), and when the processing unit encounters a loop instruction (step 400; see fig. 4; col. 8, lines 53-56), the processing unit will loop the instruction previous to the loop instruction (step 405; see fig. 4; col. 8, lines 56-57; col. 6, lines 65-67) a number of times as defined by the loop count value (see col. 2, lines 21-25).

7. Regarding claim 2, Catherwood discloses the microcomputer apparatus in claim 1 further comprising: a first memory (program memory 105, see fig. 1; col. 4, lines 25-26) coupled to the processing unit (see col. 4, lines 44-46) for storing a program (see col. 4, lines 25-26) comprising a table (REPEAT instructions)

Note that the definition of table according to The American Heritage® Dictionary of the English Language, Fourth Edition is "An orderly arrangement of data, especially one in which the data are arranged in columns and rows in an essentially rectangular form." Using this definition, a list of instructions in program memory can be considered a table.

Containing the addresses of a plurality of loop count values (see col. 7, lines 51-54).

8. Regarding claim 3, Catherwood discloses the microcomputer apparatus in claim 2 wherein the first memory is a ROM (Read Only Memory) memory (see col. 4, lines 27-28).

9. Regarding claim 4, Catherwood discloses the microcomputer apparatus in claim 2 further comprising: a program counter coupled to the processing unit (see col. 4, lines 25-26) for addressing the first memory (see col. 4, lines 57-59).

10. Regarding claim 5, Catherwood discloses the microcomputer apparatus in claim 1 wherein the processing unit comprises: an instruction decoding means (instruction fetch/decode unit 110 & loop control 135; see fig. 1; col. 4, lines 19-22) for decoding and dispatching instructions for execution (see col. 4, lines 51-53 regarding sending instructions to execution units) and for checking a loop count value (see col. 9, lines 2 -3 regarding checking whether the loop value is less than zero) stored in the loop counter

(see col. 8, lines 59-60); and an execution unit (execution units 115; see fig. 1; col. 4, lines 20-21) for executing the dispatched instructions (see col. 9, lines 8-10) and decrementing a loop count value stored in the loop counter (see col. 9, lines 1-2).

11. Regarding claim 6, Catherwood discloses the microcomputer apparatus in claim 1 wherein the loop counter comprises: a first multiplexer for selecting an address of a loop count value (see col. 8, lines 63-65 regarding specifying the address of the register that includes the loop count value),

Note that if there are many possible sources (any register) of the register, there must be a device to choose which value is used. The device used to address the register file is considered to be the first multiplexer. Further note that the definition of multiplexer according to the WordNet ® 2.0, © 2003 Princeton University is "a device that can interleave two or more activities".

A second multiplexer for determining whether a loop count value is being sent from the processing unit (step 425; see col. 9, lines 1-2 regarding storing the decremented value into the repeat count register)

Note that something must decrement the loop value. This item is considered to be part of the processing unit.

Or from the address of a loop count value (step 410, see col. 8, lines 59-60 regarding loading the repeat count register with a loop value);

Note that there are two different values that can be loaded into the count register (the value currently in the register - 1 and the new value). Using the same definition of multiplexer as used above, there must be a multiplexer to choose which value to use.

And a fourth memory (rcount register 340, see fig. 3) for storing a loop count value (see col. 7, lines 47-48) and issuing the current state of the loop count value to the processing unit (the data must be sent to a subtracter in order to decrement the value); wherein the processing unit will decrement the loop count value (see col. 9, lines 1-2) each time an instruction has been looped and will continue looping the instruction until the loop count value has reached 0 (col. 9, lines 2-3 & 6-11).

12. Regarding claim 7, Catherwood discloses the microcomputer apparatus in claim 6 wherein the fourth memory is a loop count register (rcount register 340 is a register which is used to store a loop count).

13. Regarding claim 8, Catherwood discloses the microcomputer apparatus in claim 1 wherein the computer apparatus further comprises a storage unit (memories 145, 105, W REGISTERS, and 120) coupled to the processing unit and the loop counter (all memories are coupled to all parts of processor 100, see fig. 1).

14. Regarding claim 9, Catherwood discloses the microcomputer apparatus in claim 8 wherein the storage unit further comprises: a second memory (program memory 105; see fig. 1) coupled to the processing unit and the loop counter (see col. 4, lines 44-50)

for storing a table containing the addresses of a plurality of loop count values (see above regarding claim 2); and a third memory (repeat value registers 335 and similar registers; see fig. 3) coupled to the loop counter (see col. 7, lines 51-54) for storing a plurality of loop count values (since they are addressable, multiple registers can store values to be loaded into the RCOUNT register 340).

15. Regarding claim 10, Catherwood discloses the microcomputer apparatus in claim 9 wherein the third memory is a set of registers (any memory in processor 100 is inherently a set of registers).

Note that the definition of the word register according to The American Heritage® Dictionary of the English Language, Fourth Edition is "A part of the central processing unit used as a storage location." According to this definition, any memory in a processor can be considered to be a register.

16. Regarding claim 11, Catherwood discloses the microcomputer apparatus in claim 9 wherein the second memory is a RAM (Random Access Memory) memory (see col. 4, line 35).

17. Regarding claim 12, Catherwood discloses a microcomputer apparatus comprising: a processing unit for executing instruction (execution units 115; see fig. 1); a second memory (program memory 105; see fig. 1), coupled to the processing unit, for storing a table containing addresses of a plurality of loop count values (see above

regarding claim 2); a third memory, for storing the plurality of loop count values (repeat value registers 335 and similar registers; see fig. 3); and a loop counter (repeat count register; see col. 2, lines 64-66), coupled to the processing unit, the second memory and the third memory, for receiving and storing a loop count value (see col. 8, lines 59-60) from the third memory by an address read from the second memory according to a loop instruction executed by the processing unit (see col. 8, lines 59-63); wherein the processing unit will loop a target instruction corresponding to the loop instruction a number of times as defined by the loop count value (see col. 2, lines 21-25).

18. Regarding claim 13, Catherwood discloses the microcomputer apparatus of claim 12 further comprising: a first memory (External memory 145; see fig. 1), coupled to the processing unit, for storing a program comprising the table containing the addresses of the plurality of loop count values (see above regarding claim 2); wherein the second memory loads the table containing the addresses of the plurality of loop count values from the first memory (see col. 4, lines 35-37).

19. Regarding claim 14, Catherwood discloses the microcomputer apparatus of claim 12 wherein the target instruction is previous to the loop instruction (col. 6, lines 65-67).

Response to Arguments

20. Applicant's arguments filed 21 May 2006 have been fully considered but they are not persuasive.

21. Applicant states:

> Catherwood et al. teach methods for relieving the limitation of executing a target instruction a limited number of times due to limited storage capacity for a loop count value. Specifically, Catherwood et al. disclose in col. 8, lines 59-60, "...the processor stores a loop count value into a repeat count register." Although the utilization if the repeat count register provides for increased looping capacity, it does not offer any processor cycle savings or efficiency improvements because the REPEAT instruction has to be executed prior to the target instruction (col. 3, lines 58-60). The applicant provides a dedicated loop counter as well, and additionally the claimed invention proceeds to loop the preceding instruction (col. 3, lines 58-60). The applicant provides a dedicated loop counter as well, and additionally the claimed invention proceeds to loop the preceding instruction, i.e., the instruction just prior to the loop instruction (see Step 170 in paragraph [0031]) and furthermore in paragraph [0040], "Using a loop process, the program would list instruction A first followed by a loop instruction... because instruction A is listed first, the processing unit will have already fetched instruction A before reaching the loop instruction. Consequently, when the processing unit executes the loop instruction in the second cycle, instruction A has already been fetched. As a result, the processing unit in the second cycle can execute both the loop instruction and the instruction A. "Therefore, the processing unit requires only 1 cycle for each execution of instruction A and for a total of, for example, X repetitions, X cycles are needed. Regarding the prior art, and specifically, Catherwood et al, an instruction to be looped (i.e. repeated) X times requires X+1 processor cycles.
>
> Applicant maintains that the claimed feature "the processing unit will loop the instruction previous to the loop instruction a number of times as defined by the loop count value" is not taught or suggested by Catherwood et al. Applicant further maintains that this feature of the claimed invention is not obvious for a person of ordinary skill in the art in view of the teachings of Catherwood et al. The rejection under 35 U.S.C. 102(e) is overcome accordingly. Applicant respectfully requests reconsideration of claim 1.

Examiner disagrees. As cited in the previous office action "Catherwood discloses... the processing unit will loop the instruction previous to the loop instruction (step 405; see fig. 4; col. 8, lines 56-57; col. 6, lines 65-67) a number of times as defined by the loop count value (see col. 2, lines 21-25)." Catherwood clearly states that "[t]he repeat instruction may follow the target instruction" and that "[t]he repeat instruction may specify an immediate operand specifying a loop count value corresponding number of times that the loop is to be repeated." Applicant's arguments merely state the motivation for having the repeat instruction follow the target instruction. The fact that Catherwood et al. do not disclose motivation for doing this is irrelevant.

22. Regarding new claims 12-14, see the rejection above. Note that as stated in the prior office action, Catherwood discloses a program memory comprising a table (see above regarding claim 2). Applicant merely describes how the invention operates and does not argue the validity of the original rejection of claim 2.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 7/25/06

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